Direct-Synthesis Design Technique for Nonlinear Microwave Circuits

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***Abstract*— A novel design technique for the direct synthesis of large-signal microwave circuits is presented. It is based on an equivalent linear representation of the nonlinear circuit directly derived from an exact nonlinear analysis method, e.g., of the harmonic balance type. Linear, direct sysnthesis methods are then applied to this equivalent network. The drawbacks of nonlinear optimization are so avoided, while keeping the advantages of exact nonlinear analysis and accurate nonlinear models.**

I. Introduction

MODERN MICROWAVE systems include several types of nonlinear circuits, as power amplifiers, mixers, oscillators and frequency multipliers. The final cost and performances of the system heavily depend on the availability of efficient and accurate design techniques and procedures, that allow the designer to perform his task in the shortest possible time with good simulation accuracy. To this goal nonlinear models and analysis methods are vital to accurately simulate the behavior of the circuits prior to fabrication, and to save costly and time-consuming production iterations. Nowadays accurate and powerful nonlinear CAD packages and models are commercially available, for the simulation of microwave nonlinear circuits [1]–[4]; however, they usually are not specifically addressed to the design. On the other hand, several simplified methods have been proposed for very fast design of specific ciruits like power amplifiers or mixers [5], [9], but they lack accuracy because of their basic simplifying assumptions on the nonlinear device. In this paper we propose a method that, making use of full nonlinear model and analysis algorithm (of the harmonic balance type), defines a linear equivalent circuit valid in large-signal conditions. On this circuit direct synthesis techniques are applied, in the same way as in actual linear circuits, avoiding the application of nonlinear optimization procedures. The accuracy of the method is that of the basic nonlinear analysis, but design conditions (as for instance conjugate matching) can be directly applied, with the advantages of clarity and speed; the results are obviously valid for large-signal conditions. The basic features of the method together with examples of applications to typical nonlinear circuits are presented in the following.

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II. The Nonlinear Design Method

Following standard nonlinear analysis methods [6] the circuit can be first divided into linear and nonlinear subnetworks, connected by a number $(N+1)\cdot M$ of electrical ports, representing the N harmonics, plus DC, of the voltages and currents at the M physical connecting ports. For the linear subnetwork a matrix representation is immediately defined in frequency domain, e.g., an admittance matrix Y_L, together with a vector of sources, representing the external excitations. The actual sources are usually replaced by equivalent ones at the (electrical) connecting ports, e.g., Norton equivalent current sources. The nonlinear subnetwork is usually analysed in time domain: a time-domain voltage waveform vector $v(t)$ is applied, and a current waveform vector $i_{NL}(t)$ is computed in the time domain as a function of applied voltages. Connection with the frequency-domain analysis of the linear subnetwork is provided by Fourier transform.

Equating the linear and nonlinear currents simultaneously at all ports, as required by Kirkhhoff's law, yields the system of the harmonic-balance equations, where the unknowns are the voltages at the same ports

$$I_L = I_{0,L} + Y_L \cdot V \quad \text{linear sub-network} \tag{1}$$

$$i_{NL}(t) = f[v(t)]; \quad I_{NL} = \mathcal{T}\{i_{NL}(t)\} \quad \text{non-linear sub-network} \tag{2}$$

$$g(V) = I_L + I_{NL} = 0 \quad \text{harmonic-balance system.} \tag{3}$$

The system is obviously nonlinear in the unknown V, and must be solved with a zero-searching iterative method. The Newton-Raphson algorithm is usually employed, that requires the computation of the derivative $J(V) = \partial g(V)/\partial V$ (the Jacobian matrix) of the system equations $g(V)$ with respect to the unknown voltages V. When the Newton-Raphson algorithm finally reaches convergence, the voltage V is the actual large-signal voltage present in the circuit. So far, the described analysis is pretty standard.

We now consider that the computation of the Jacobian requires the evaluation of the derivative of the nonlinear currents with respect to the applied voltages $\partial I_{NL}/\partial V$, that can be regarded as an equivalent admittance matrix of the nonlinear subnetwork. In the Jacobian of the last iteration of the Newton-Raphson algorithm, the applied voltages are the solution of the system, i.e., the actual voltages in the nonlinear circuit, and the equivalent admittance matrix represents the effect of an actual

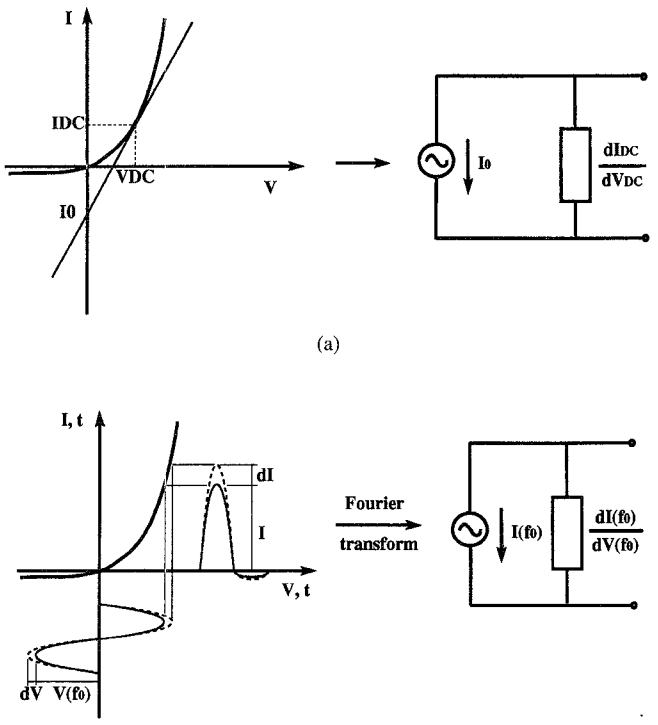

Fig. 1. (a) Linear large-signal equivalent network of a diode at zero-frequency (DC). (b) Linear large-signal equivalent network of a diode at non-zero-frequency.

voltage perturbation on the nonlinear subnetwork under large-signal drive. A linear equivalent "incremental" representation is therefore available for the nonlinear subnetwork, at no additional computational cost. Similar considerations have been already used [7] and [8] for sensitivity analysis or for optimization purposes, but no use of them has been done for direct circuit synthesis.

To the purpose of obtaining not just a perturbation or gradient, but a completely equivalent network, in fact, equivalent current sources must be added: they are easily computed from the available data, in the same way as for the linear subnetwork. In Fig. 1(a) an example of this principle is shown for a simple diode for the zero-frequency harmonic (DC); in Fig. 1(b) the same is shown for a non-zero-frequency harmonic. In the former case the origin of the equivalent current source and admittance is clear: a small perturbation of the DC bias generates an incremental current along the differential admittance around the bias point. In the latter case the role of the DC bias voltage is played by the large-signal "bias" sinusoid; the small perturbation, i.e., the small variation in amplitude or phase of the sinusoid, generates a change of the large-signal current waveform, from which the relevant frequency component is extracted through a Fourier analysis. The ratio between the voltage and current variations is the incremental admittance. Equation (2) can now be rewritten as

$$I_{NL} = I_{0,NL} + \left(\frac{\partial I_{NL}}{\partial V}\right) \cdot V = I_{0,NL} + Y_{NL} \cdot V$$

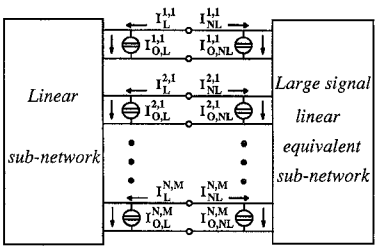

Fig. 2. The linear equivalent network of the complete circuit.

in analogy with (1). In this way the complete network is now composed by the (fictitious) equivalent current generators and by the equivalent admittances at all ports and frequencies, and is overall equivalent to the actual nonlinear circuit (Fig. 2); obviously, the validity of the representation is limited to a neighborhood of the working point.

This equivalent representation is used for a direct synthesis of the circuit with linear methods. The embedding linear network can be synthesized to fulfill a design criteria, as for instance conjugate match for maximum power gain. Of course, if the synthesis leads the circuit away from the operating point, a new nonlinear analysis is required: the linear equivalent representation is in fact valid at a fixed drive level, bias point, and loading. A new equivalent representation must be therefore computed if the loading impedances are varied; usually, however, only two or three iterations are required to reach the final and correct circuit. It is worth reminding that the voltages and currents present in this equivalent linearized circuit are the actual large-signal ones, and that consequently large-signal quantities as DC or RF power, power gain, conversion gain, rectified DC current, voltage and current waveforms, and so on, are directly computed from the linear circuit. The proposed technique is therefore a valid alternative to nonlinear optimization methods.

III. Examples and Applications

The presented general technique has been applied to several examples. As mentioned above, the electrical ports represent all the harmonic frequency components of all the physical ports of the active component; any nonlinear circuit, including strongly nonlinear ones as multipliers and harmonic-reaction power amplifiers, can therefore be accurately designed.

A typical application is the design of power amplifiers. Large-signal design conditions are conjugate match at the input and resistive loading of the controlled current source of the transistor at the output [9]–[11] for maximum power gain at fundamental frequency; low and high impedance at even and odd harmonics respectively for maximum efficiency [12], [11]. A high-efficiency power amplifier with harmonic loading has been studied with the aid of the described linear representation [11]. The active device is a 27 dBm, 0.5 μm power MESFET from GMMT; the operating frequency is 5 GHz. The nonlinear model for the transistor is a modified Materka one based on RF and pulsed measurements for class-AB applications [13]. As said before, the design conditions at fundamental frequency are conjugate match at the input and resistive loading of

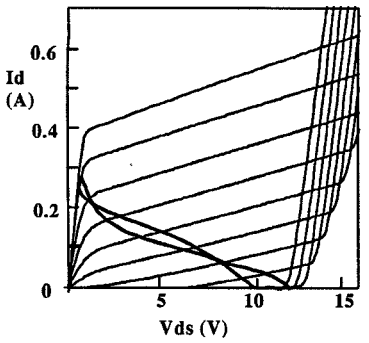

Fig. 3. Load curve of an optimized class-AB power amplifier.

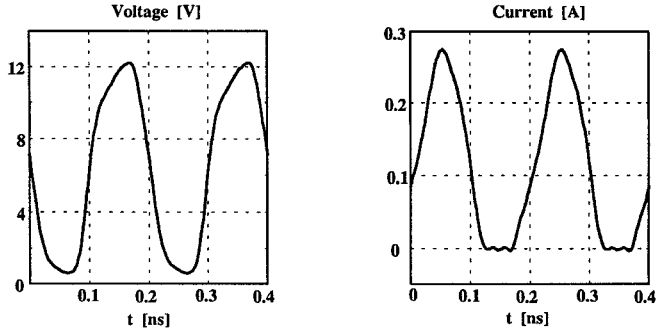

Fig. 4. Drain voltage and current waveforms of an optimized class-AB power amplifier.

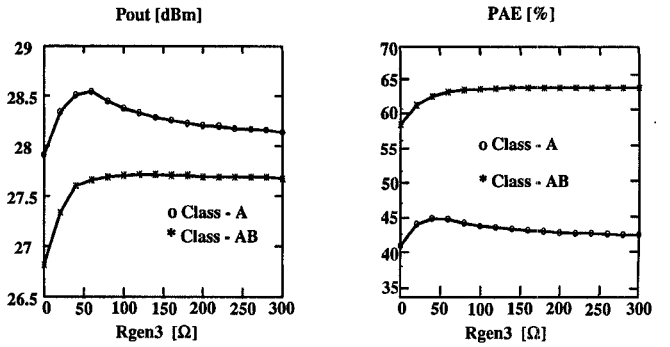

Fig. 5. Output power and power-added efficiency of a class-AB power amplifier versus third harmonic load.

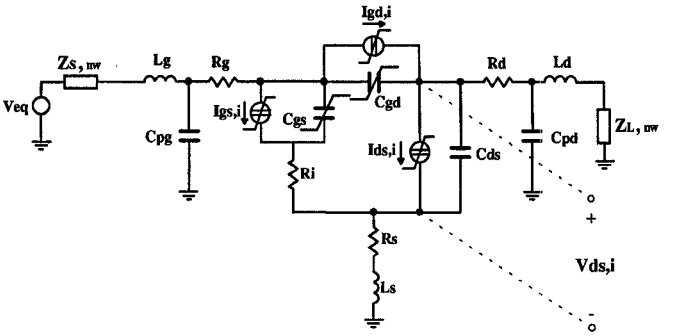

Fig. 6. The schematic of a frequency doubler, where $Z_{S,n\omega} = \begin{cases} Z_{S,1} & n=1 \\ X_{S,2} & n=2 \\ 0 & n>2 \end{cases}$ $Z_{L,n\omega} = \begin{cases} X_{L,1} & n=1 \\ R_{L,2}+jX_{L,2} & n=2 \\ 0 & n>2 \end{cases}$ and $Z_{\mathrm{gen},n\omega} = \dfrac{V_{ds,i}(n\omega)}{I_{ds,i}(n\omega)}$ $n = 1, 2, \cdots$.

the drain-source current generator at the output, under large-signal drive. While the nonlinear harmonic-balance analysis includes ten harmonics, only second- and third-harmonic loads have been considered available to the designer because of technological limitations, while upper harmonics have been considered as practically shorted by the intrinsic output shunt capacitance of the transistor. The second-harmonic load has been imposed to be a short circuit [12], while the third-harmonic load has been left as a free parameter for maximum efficiency design. The output curve of the designed class-AB stage are shown in Fig. 3, corresponding to the drain voltage and current waveforms of Fig. 4. An efficiency of more than 60% is obtained, due to the optimized shape of the output waveforms. The design has been done with our in-house program on an 80486 PC in less than one minute. Given the efficiency of the method, the power and efficiency performances for varying third-harmonic loading have been studied in a very short computer time, and are shown in Fig. 5 for class-A and AB operations: it is to note that each point corresponds to repeated analysis/optimization procedures and do not correspond to a single linearization of the active device.

Another example is the design of an active frequency doubler. In this case the quantities to maximize are the second-harmonic output power and/or the conversion gain for a fixed input power. The schematic of the circuit is shown in Fig. 6, where the embedding network to be designed includes input and output first- and second-harmonic loads. The design conditions imposed to the linear equivalent circuit for maximum power gain are conjugate input match at fundamental frequency and resistive loading of the controlled current source at second harmonic under large-signal drive, as already seen in the case of the power amplifier. Input impedance at second harmonic $X_{S,2}$ and output impedance at fundamental frequency $X_{L,1}$ must be reactive, in order to minimize losses and to increase the isolation of the power source and of the load [14], [15]. The value of the latter reactance is determined by imposing a maximum voltage swing at the input, under large-signal drive on the linear equivalent circuit; the former is left as a free parameter for maximum conversion gain. The same MESFET and nonlinear model as in the power amplifier design have been used for a 5–10 GHz doubler, with the transistor biased near pinch-off. In Fig. 7 the load curve, and in Fig. 8 the corresponding input voltage and output voltage and current waveforms for an optimized circuit are shown. In Fig. 9 the real and imaginary parts of the optimized input matching impedance are shown versus input power, illustrating the effect of the nonlinearities under large-signal drive. In Fig. 10 the conversion gain is plotted versus the resistive load at second harmonic $R_{\mathrm{gen},2}$, with input reactance at second harmonic $X_{S,2}$ as a parameter, for three different input power levels. The plots have been obtained in a few minutes with our in-house program on an 80486 PC. As can be clearly noted, well defined conversion gain maxima are present in the plots, corresponding to output power maxima; a strong influence of $X_{S,2}$ suggests for it a careful control. A minor influence of $R_{\mathrm{gen},2}$ is also apparent.

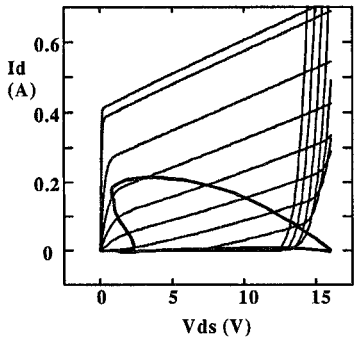

Fig. 7. Output curve of an optimized frequency doubler.

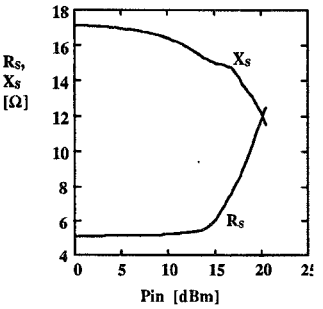

Fig. 9. Real and imaginary parts of the matching impedance of the frequency doubler versus input power

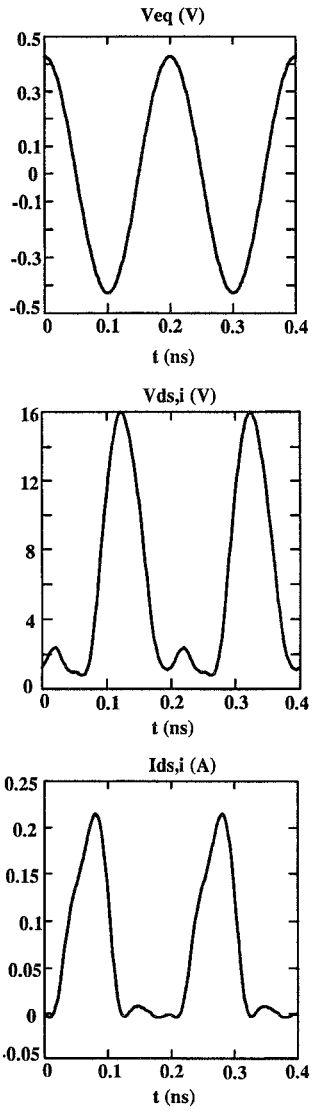

Fig. 8. Input voltage, output voltage and current waveforms of an optimized frequency doubler.

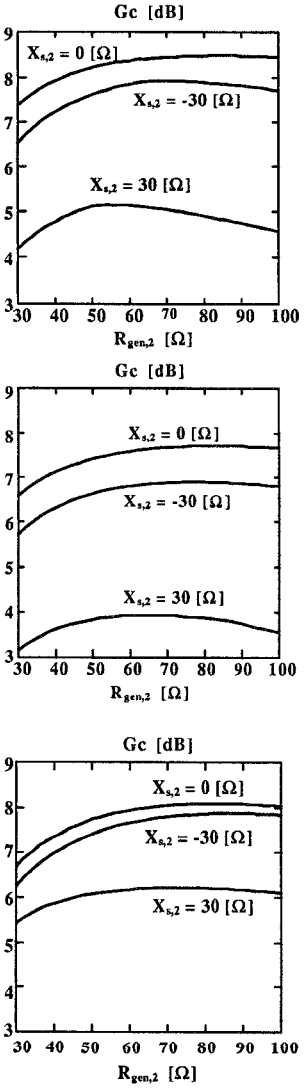

Fig. 10. Conversion gain of the frequency doubler versus second-harmonic load, with second-harmonic input reactance as a parameter.

These results obviously have the same accuracy of standard nonlinear CAD analyses, since a complete nonlinear model and an exact nonlinear analysis method have been used. The design time is however much lower, because the design conditions have been directly imposed on the large-signal linear equivalent circuit, consistently with the nonlinear analysis. Plots or charts are then very quickly generated, for the choice of design trade-offs. This is a crucial point: design trade-offs, in fact, are not clearly visible after a standard nonlinear optimization, which leads, in the hypothesis of convergence, to a single solution. On the other hand, much like in the case of linear

synthesis methods (as for instance the trade-off between noise figure and gain), with the proposed direct synthesis technique all possible solutions and alternatives are clearly and quickly available to the designer.

IV. Conclusion

A novel design technique has been described for the direct synthesis of nonlinear microwave circuits. The procedure is based on the use of an exact nonlinear analysis method of the harmonic-balance type, from which a linear equivalent representation, valid under large-signal conditions, is extracted. The synthesis of the embedding network is then performed with the usual methods for linear circuits, without optimization. This general technique has been applied to the design of a high-efficiency power amplifier and of a frequency doubler; a computer program has been written to this purpose, that runs very efficiently on a PC. The resulting procedure is very fast, and easily interpreted by the designer.

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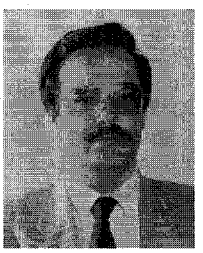

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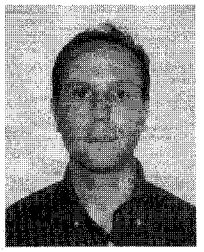

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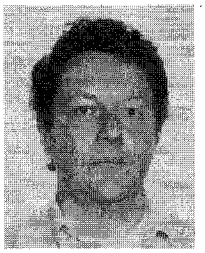

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